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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,832	10/30/2003	Alain Blanc	FR920020089US1	9274
25299	7590	05/18/2005	EXAMINER	
IBM CORPORATION PO BOX 12195 DEPT 9CCA, BLDG 002 RESEARCH TRIANGLE PARK, NC 27709			LE, TOAN M	
			ART UNIT	PAPER NUMBER
			2863	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/697,832

Applicant(s)

BLANC ET AL.

Examiner

Toan M. Le

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 9-21 are rejected under 35 U.S.C. 102(b) as being anticipated by “Automatic Distortion Correction for Efficient Pulse Transmission”, Schreiner et al (referred hereafter Schreiner et al.).

Referring to claim 1, Schreiner et al. disclose a method for automatically adjusting parameters of signal emitter of a synchronous high-speed transmission system wherein controller of signal receiver could transmit information to the controller of the signal emitter (Abstract), the method comprising:

selecting a first subset of values in a predetermined set of values;

sending a request to the controller of the signal emitting means for setting the parameters to the values of the selected subset (page 22, 1st col., lines 16-18; figure 4);

evaluating the quality of the signal received by the signal receiver (page 22, 1st col., lines 16-18);

if all subsets of the predetermined set of values have been selected, determining the subset corresponding to the best signal quality and sending a request to the controller of the signal emitter for setting the parameters to the values of the determined subset (page 22, 1st col., lines 16-31).

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As to claim 2, Schreiner et al. disclose a method for automatically adjusting parameters of signal emitter of a synchronous high-speed transmission system wherein controller of signal receiver could transmit information to the controller of the signal emitter wherein the evaluating the quality of the received signal comprises over-sampling the received signal to determine positions of signal transitions (page 24, 1st col., 1st and 2nd paragraphs).

Referring to claim 3, Schreiner et al. disclose a method for automatically adjusting parameters of signal emitter of a synchronous high-speed transmission system wherein controller of signal receiver could transmit information to the controller of the signal emitter wherein the receiver comprises a sampler controlled by a phase rotator, the evaluating the quality of the received signal comprising analyzing the behavior of the phase rotator (page 21, 1st col., last paragraph and 2nd col., 3rd, 4th, and 5th paragraphs).

As to claim 4, Schreiner et al. disclose a method for automatically adjusting parameters of signal emitter of a synchronous high-speed transmission system wherein controller of signal receiver could transmit information to the controller of the signal emitter wherein the receiver comprises a sampler controlled by a phase rotator, the evaluating the quality of the received signal comprising determining a digital eye, the digital eye characterizing the position whereat transitions of the received signal have been detected (page 22, 2nd col., 1st paragraph; page 23, 2nd col., 1st paragraph; figures 8-9).

Referring to claim 9, Schreiner et al. disclose a program product including:

a computer readable medium;

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a computer program disposed on the computer readable medium, the computer program including a first instruction set that generates sub-sets of parameter values in a predefined set of parameter values (page 22 to page 23, Fundamental considerations section); and

a second set instruction set to select sub-set of parameter values to be used as parameter values for a signal generating emitter (page 24, 1st col., lines 3-30).

As to claim 10, Schreiner et al. disclose a method comprising:

generating a signal by a signal emitter whose parameter values are being set to at least two different sub-sets of values (page 22, 1st col., lines 26-31; figure 4);

evaluating the quality of the signal, with a signal analyzer, as each set of the at least two different sub-sets of parameter values are being applied (page 22, 1st col., lines 16-31); and

setting the parameter values of the signal emitter to the sub-set of parameter values providing best quality of signal (page 22, 1st col., lines 16-31).

Referring to claim 11, Schreiner et al. disclose a method wherein evaluating includes generating a digital eye based upon oversampling of the signal (page 22, 2nd col., 1st paragraph; page 23, 2nd col., 1st paragraph; figures 8-9).

As to claim 12, Schreiner et al. disclose a method wherein the best quality of signal is being determined from the digital eye (page 22, 2nd col., 1st paragraph; page 23, 2nd col., 1st paragraph; figures 8-9).

Referring to claim 13, Schreiner et al. disclose a method wherein the evaluating further includes providing a phase rotator to sample the signal (page 21, 1st col., last paragraph and 2nd col., 3rd, 4th, and 5th paragraphs).

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As to claim 14, Schreiner et al. disclose a method wherein behavior of the phase rotator is used to determine quality of the signal (page 21, 1st col., last paragraph and 2nd col., 3rd, 4th, and 5th paragraphs).

Referring to claim 15, Schreiner et al. disclose a method further including generating a digital eye by moving the phase rotator to different positions within a beginning location and an end location; and sampling data at each position (figures 8-9).

As to claim 16, Schreiner et al. disclose a method wherein the quality of signal is being determined from the digital eye (page 22, 2nd col., 1st paragraph; page 23, 2nd col., 1st paragraph; figures 8-9).

Referring to claim 17, Schreiner et al. disclose a program product further including a third instruction set which analyzes a signal generated by the signal generating emitter; and a fourth instruction set identifying the sub-set of parameter values that generate the signal with best quality (page 24, 1st col., lines 28-40).

As to claim 18, Schreiner et al. disclose an apparatus that automatically determines parameter values for a signal emitter comprising:

a first controller responsive to a request signal to provide different sub-sets of parameter values to the signal emitter (figure 4; page 22, 1st col., lines 14-31); and

a second controller generating the request signal, evaluating quality of signal generated by the signal emitter and selecting the sub-set of parameter values providing the best quality of signal (page 22, 1st col., lines 14-31).

Referring to claim 19, Schreiner et al. disclose an apparatus that automatically determines parameter values for a signal emitter further including a communication channel interconnecting the first controller and the second controller (figure 4).

As to claim 20, Schreiner et al. disclose an apparatus that automatically determines parameter values for a signal emitter further including the second controller sending a second request instructing the first controller to set parameter values of the emitter to the sub-set of parameter values providing best quality of signal (page 2, 1st col., lines 14-31).

Referring to claim 21, Schreiner et al. disclose an apparatus that automatically determines parameter values for a signal emitter wherein the first controller and the second controller includes microprocessors (figure 4).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

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1. A method for analyzing the quality of a high speed signal comprising:
 setting said phase rotator in a first position;
 initializing a partial value associated to said phase rotator position;
 sampling said high speed signal;
 XORing said sample and said sample shifted by 1 bit;
 ORing the result of said XOR operation with said partial result associated to said phase rotator position;
 replacing the value of said partial result associated to said phase rotator position by the result of said OR operation;
 repeating the last four acts during a predetermined time;
 setting said phase rotator in a second position and repeating the last six acts; and,
 combining said partial results associated to said first and second positions.

2. The method of claim 1 wherein the phase rotator is set to all its possible positions, a partial result being determined for each position of said phase rotator, and the quality of said high speed signal is characterized by the combination of said partial results.

3. The method of either claim 1 or claim 2 wherein combining said partial results comprises:
 emptying a value characterizing the quality of said high speed signal, setting a bit position to the number of bits of said partial results and setting a phase rotator position value to the value of the first position reached by said phase rotator;
 selecting the bit of the partial result associated to said phase rotator position value, located at said bit position;
 merging said selected bit to said value characterizing the quality of said high speed signal;
 if said selected bit is part of the partial result associated to the last position of said phase rotator,
 if said selected bit is the first bit of the partial result, ending said combining step;
 else, decreasing said bit position by one, setting said phase rotator position value to the value of the first position reached by said phase rotator and repeating the last four acts;
 else, increasing said phase rotator position value by one and repeating the last five acts.

6. The method of claim 5 wherein said correcting said value characterizing the quality of said high speed signal comprises:
 if said shifting is a right shifting, suppressing a number n of consecutive bits equal to one, from the right, for each set of consecutive bits equal to one; or,
 if said shifting is a left shifting, suppressing a number n of consecutive bits equal to one, from the left, for each set of consecutive bits equal to one, wherein n is the number of position reached by said phase rotator, minus one.

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5. The method of claim 4 wherein said digital eye is determined by:
 setting said phase rotator in a first position;
 initializing a partial value associated to said phase rotator position;
 sampling the received signal;
 XORing said sample and said sample shifted by 1 bit;
 ORing the result of said XOR operation with said partial result associated to said phase rotator position;
 replacing the value of said partial result associated to said phase rotator position by the result of said OR operation;
 repeating the last four steps during a predetermined time;
 setting said phase rotator in a second position and repeating the last six steps; and,
 combining said partial results associated to said first and second positions.

6. The method of claim 5 wherein the phase rotator is set to all its possible positions, a partial result being determined for each position of said phase rotator, and said digital eye being determined by the combination of said partial results.

7. The method of claim 5 wherein said step of combining said partial results comprises the steps of:
 emptying a value representing the digital eye, setting a bit position to the number of bits of said partial results and setting a phase rotator position value to the value of the first position reached by said phase rotator;
 selecting the bit of the partial result associated to said phase rotator position value, located at said bit position;
 merging said selected bit to said value representing the digital eye;
 if said selected bit is part of the partial result associated to the last position of said phase rotator,
 if said selected bit is the first bit of the partial result, ending said combining step;
 else, decreasing said bit position by one, setting said phase rotator position value to the value of the first position reached by said phase rotator and repeating the last four steps;
 else, increasing said phase rotator position value by one and repeating the last five steps.

8. The method of claim 5 further comprising correcting the digital eye:
 if said shifting is a right shifting, suppressing a number n of consecutive bits equal to one, from the right, for each set of consecutive bits equal to one; or,
 if said shifting is a left shifting, suppressing a number n of consecutive bits equal to one, from the left, for each set of consecutive bits equal to one, wherein n is the number of position reached by said phase rotator, minus one.

Claims 5-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3 and 6 of copending Application No. 10/697,495. Although the conflicting claims are not identical, they are not patentably distinct from each other because the digital eye is represented/equivalent a high-speed signal via a scope illustrated by Schreiner et al. reference so that it would have been obvious to one having ordinary skill in the art at the time the invention was made to have applied a scope for displaying the high-speed signal for adjusting parameters of the emitter to optimize the high-speed signal transmission.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

“Adjustment of Predetection Filters in High-Speed Data Transmission Systems”,
Bateman et al., IEE Proceedings, Vol. 137, Pt. I, No. 6, December 1990, Pages 355-364

“A Low-Power 8-PAM Serial Transceiver in 0.5- μ m Digital CMOS”, Foley et al., IEEE
Journal of Solid-State Circuits, Vol. 37, No. 3, March 2002, Pages 310-316

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan M. Le whose telephone number is (571) 272-2276. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M..

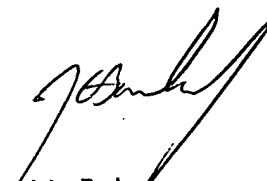
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Toan Le

May 3, 2005



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